**Assignment 1:**

1. Give a formal or descriptive definition for each of the following terms.

* ITRS,
* IRDS，
* Gate-Equivalent,
* Technology Nodes,
* Feature size,
* IC design complexity sources,
* Behavioral representation,
* Abstraction hierarchy,
* IC design,
* Synthesis,
* Refinement,
* System-level synthesis,
* Logic synthesis,
* Layout synthesis,
* Digital design space,
* Static timing analysis,
* Behavioral simulation,
* Post place and route simulation,
* Design Technology Co- Optimization (DTCO),
* Mask synthesis.

1. Access the Internet for information about Daniel D. Gajski’s “Y-chart” methodology for integrated circuits design. According to your investigation of the related research papers and/or technical reports, please summarize the “Y-chart” theory, including

(1) design representation domains,

(2) design abstraction hierarchy and

(3) design activities.

References must be listed at the end of your report.

1. Write a summary *in Chinese* of the paper “*A New Ear in Advanced IC Design*” (in less than 200 characters).

**Answer:**

1. Give a formal or descriptive definition for each of the following terms.

* **ITRS:**International Technology Roadmap for Semiconductors
* **IRDS:**International Roadmap for Devices and Systems
* **Gate-Equivalent:**A basic unit used to describe the complexity of a circuit design which is independent of manufacturing technology.Corresponds to a two-input NAND gate
* **Techn****ology Node****s:**It refer to specific process technology milestones that indicate the size of the smallest feature that can be reliably manufactured on a chip
* **Feature size:**The minimum line width in the device (in MOS devices, the feature size refers to the channel length determined by the device gate electrode)
* **IC design complexity sources:**Large chip size,Variability and reliability,Power dissipation,and Heterogeneity
* **Behavioral represent****ation:**Behavior represents a design as a black box and describes its outputs in terms of its inputs and time.The black-box behavior indicates no geometrical information or structural information.Behavior takes the form of textual, mathematic or algorithmic description
* **Abstraction hierarchy:**A set of interrelated representation levels that allow a system to be represented in varying amounts of detail
* **IC design:**A large number of devices and interconnects are placed on a piece of semiconductor substrate material (usually silicon), and the circuit is designed on this basis
* **Synthesis:**The process of transforming one representation in the design abstraction hierarchy into another representation. (Synthesis = Translation + Optimization)
* **Refinement:**The process of converting information directly from the behavioral domain to the geometric domain
* **System-level synthesis:**Mapping a task-level specification onto a heterogeneous hardware / software architecture
* **Logic synthesis:**Translation from a dataflow representation to a structural logic gate representation.
* **Layout** **synt****hesis:**Translation from logic gate representation to layout representation.
* **D****igital design space:**Including three typical axes: area, speed, cost
* **Static timing analysis:**It analyses logic by computing the delay times for each path according to the timing model. It requires no test vectors.
* **Behavioral simulation:**This type of simulation is performed early in the design process to verify the functionality of the design at a high level. It focuses on the logic and algorithms without considering the physical implementation details
* **Post place and route simulation:**This simulation occurs after the design has been synthesized, placed, and routed. It aims to verify the timing and functional correctness of the IC with a layout that reflects actual physical design
* **Design Technology Co- Optimization (DTCO):**DTCO is a methodology that helps semiconductor fabs reduce cost and time-to-market in advanced process development.
* **Mask synthes****is:**Mask synthesis is comprised of lithographic tools for both development and batch use models, performing full-chip optical proximity correction (OPC), inverse lithographic techniques (ILT), and process checking and analysis on post-corrected IC layout patterns

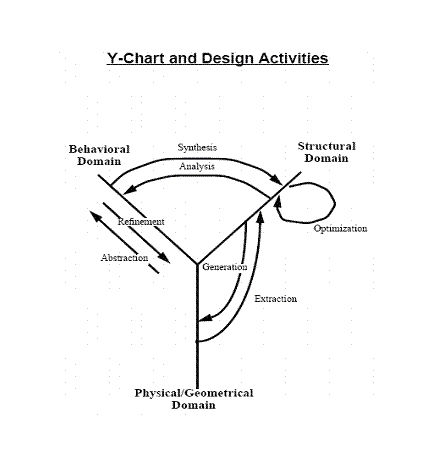
1. (1) design representation domains:Including three domains:

**Behavioral (Functional) Representation (BR):**Behavior represents a design as a black box and describes its outputs in terms of its inputs and time.The black-box behavior indicates no geometrical information or structural information.Behavior takes the form of textual, mathematic or algorithmic description.

**Structural Representation (SR):**A black box is represented as a set of components and connections. It acts as a bridge between functional representation and geometrical representation. No physical information is contained - parameters, such as size and position.

**Geometrical Representation (GR):**It specifies size (height and width), the position of each component, each port and connection on the silicon substrate or board. Geometrical shapes represent regions of diffusion, polysilicon, and metal on the silicon surface, etc..It includes mask information in layout file. This file is used to make masks of ICs.It is the lowest level of design abstraction.

1. **design abstraction hierarchy:**A set of interrelated representation levels that allow a system to be represented in varying amounts of detail.It includes six levels: System level,Chip/Behavior Algorithm level,Register Transfer Level (RTL),Logic Gate Level,Circuit Level,Layout/Silicon level.
2. **design activities:**Including six activities: Synthesis, Analysis, Refinement, Abstraction, Extraction, Generation.The relationship between activities and domains is shown in the following figure:



The common synthesis steps include:

* **Natural language synthesis:**transformation from one form of design represented by one natural language (English, for example) to an algorithmic representation.
* **System-level synthesis:**mapping a task-level specification onto a heterogeneous hardware / software architecture.
* **Algorithmic synthesis (behavioral synthesis):**translation from an algorithmic representation to a dataflow representation (or to a gate-level representation).
* **Logic synthesis:**translation from a dataflow representation to a structural logic gate representation.
* **Layout synthesis:**translation from logic gate representation to layout representation.
* **Physical synthesis:**creating a properly place-and-routed circuit from RTL code.

**References:**

1. Gajski and Kuhn, "Guest Editors' Introduction: New VLSI Tools," in Computer, vol. 16, no. 12, pp. 11-14, Dec. 1983, doi: 10.1109/MC.1983.1654264.

3. Write a summary *in Chinese* of the paper “*A New Ear in Advanced IC Design*” (in less than 200 characters).

目前的IC设计流程存在一系列挑战：IP核的专用性；多处理器导致在硅系统中建模和验证非常复杂;缺乏面向硅的嵌入式软件解决方案。

SoC将设计从创造转变为组合。与传统设计的区别包括：更多的系统级设计阶段、以SoC为中心的嵌入式软件设计、多层验证方法、咨询服务。

SoC设计的不成熟、成本和不确定性让许多设计师处于观望状态，但随着IP的可重用性提高，以及系统级设计工具和模型的出现，SoC将在未来得到广泛应用。